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10/521,881	09/28/2005	Stefan Marco Koch	CH 020024	8855
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NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER GIBROUX, GEORGE	
			ART UNIT 2183	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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ip.department.us@nxp.com

Office Action Summary

Application No.

10/521,881

Applicant(s)

KOCH ET AL.

Examiner

GEORGE D. GIROUX

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 August 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7, 9, 10 and 13-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 9, 10 and 13-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/5508)
Paper No(s)/Mail Date 17 November 2008.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- 5) ☐ Notice of Informal Patent Application.
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed 14 August 2008, in response to the Office Action mailed 14 May 2008. The applicant's remarks and amendments to the claims and specification were considered, with the results that follow.
2. Claims 8, 11 and 12 have been cancelled while new claims 13-22 have been added. Thus claims 1-7, 9, 10 and 13-22 are now pending in this application.

Information Disclosure Statement

3. As required by **M.P.E.P. 609(c)**, the applicant's submission of the Information Disclosure Statement, dated 17 November 2008, is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 13, 14, 16 and 18-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Koch (US 2002/0055979).

As per claims 13, 20 and 21, Koch teaches a first processor and a first shareable unit coupled to a first bus, the first processor and first shareable unit operating on a first processor clock as **[a first processor P1 is connected to a processor bus 40 (paragraph 0050 and figure 4) the first processor P1 on its own clock domain, P1 clock (paragraphs 0046 and 0056) and access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045), where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)]**; a second processor and a second shareable unit coupled to a second bus, the second processor and second shareable unit operating on a second processor clock as **[a second processor P2 that also has a processor bus 50 (paragraph 0050 and figure 4) the second processor P2 on its own clock domain, P2 clock (paragraphs 0046 and 0056) and access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045) where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)]**; a first bi-directional channel to couple the second processor to the first shareable unit via the first and

second busses, the first bi-directional channel configured to decouple the clock domain of the second processor from the clock domain of the first shareable unit as **[a communication channel for transferring information can be established between the first shareable unit and the second processor and between the second shareable unit and the first processor (paragraph 0051)]**, the first bi-directional channel also coupled through a first programming interface to the second processor as **[a communication channel for transferring information can be established between the first shareable unit and the second processor and between the second shareable unit and the first processor (paragraph 0051), where enhanced processor interfaces are provided for linking the processors to the common bus (paragraph 0010)]**; and a second bi-directional channel to couple the first processor to the second shareable unit via the first and second busses, the second bi-directional channel configured to decouple the clock domain of the first processor from the clock domain of the second shareable unit as **[a communication channel for transferring information can be established between the first shareable unit and the second processor and between the second shareable unit and the first processor (paragraph 0051), where an access unit decouples the data flow between the clock domain of the first processor and the clock domain of the second processor (paragraph 0056)]**, the second bi-directional channel also coupled through a second programming interface to the first processor, the second bi-directional channel being simultaneously operable with the first bi-directional channel between the first and second bus as **[each processor can access, via communication channels, the**

shareable unit and devices within the processing environment of the other processor without having to go through that processor (paragraphs 0051-0052)].

As per claims 14 and 22, Koch teaches a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock as **[DMA 41, with external interface 42, is connected to processor bus 40 via interface 44 (paragraph 0051 and figure 4) associated with the first processor clock domain, P1 clock (paragraphs 0046 and 0056)]**; a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock as **[DMA 54, with external interface 55, is connected to the processor bus 50 via interface 57 (paragraph 0052 and figure 4) associated with the second processor clock domain, P2 clock (paragraphs 0046 and 0056)]**; and a first programmable unit coupled between the first external channel of the first DMA unit and the first external channel of the second DMA unit as **[access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045), where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)]**, the first programmable unit comprising the first programming interface to the second processor, the first programmable unit also configured to decouple the second processor clock from the

first processor clock as **[access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045), where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048) and where the access units 48 and 51 decouple the data flow between the clock domain of the first processor and the clock domain of the second processor (paragraph 0056)].**

As per claim 16, Koch teaches a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock as **[DMA 41, with external interface 42, is connected to processor bus 40 via interface 44 (paragraph 0051 and figure 4) associated with the first processor clock domain, P1 clock (paragraphs 0046 and 0056)]**; a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock as **[DMA 54, with external interface 55, is connected to the processor bus 50 via interface 57 (paragraph 0052 and figure 4) associated with the second processor clock domain, P2 clock (paragraphs 0046 and 0056)]**, a first external channel of a common programmable unit, the first external channel operating on the second processor clock, and the first external channel also coupled to the first external channel of the second DMA unit and a second external channel of the common programmable

unit, the second external channel to operate on the first processor clock, and the second external channel also coupled to the first external channel of the first DMA unit as **[access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) and access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4) (where the two access units form the common programmable unit), which can each be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045) and where the access units 48 and 51 decouple the data flow between the clock domain of the first processor and the clock domain of the second processor (paragraph 0056)]**; and a first programmable core of the common programmable unit, the first programmable core to operate on the second processor clock as **[the clock signal of processor P2, P2 clock, is fed via clock line 73 to processor interface 72 of access unit 51 (paragraph 0056)]**, the first programmable core coupled between the first and second external channels of the common programmable unit and the first programmable core comprising the first programming interface to the second processor as **[access unit 51 is connected to processor P2 via processor interface 72 (paragraph 0056) which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)]**.

As per claim 18, Koch teaches wherein the first bi-directional channel further comprises a first master configured to initiate data transfers with active devices on the

first or second busses as **[a system controller is used to initiate transfers (paragraph 0063)]**.

As per claim 19, Koch teaches wherein the second bi-directional channel further comprises a second master configured to initiate data transfers with active devices on the first or second busses as **[a system controller is used to initiate transfers (paragraph 0063)]**.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-7, 9, 10, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koch (US 2002/0055979) in view of Tang (US 6,775,717).

As per claim 1, Koch teaches a first processor bus as **[a first processor bus 40 (paragraph 0050 and figure 4)]**, a first processor on a first clock connected to the first processor bus as **[a first processor P1 is connected to a processor bus 40 (paragraph 0050 and figure 4) the first processor P1 on its own clock domain, P1 clock (paragraphs 0046 and 0056)]**, a first direct memory access unit with an external direct memory access channel, and connected to the first processor bus as **[DMA 41, with external interface 42, is connected to processor bus 40 via interface 44**

(paragraph 0051 and figure 4)], a first programmable unit comprising a first processor interface coupled, via the first external direct memory access channel, to the first direct memory access unit, said first programmable unit being programmable by the first processor via the first processor interface as **[access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045), where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)],** a first shareable unit being connectable to the first processor bus as **[shareable unit 43 connected to processor bus 40 (figure 4)],** a second processor bus as **[the second processor bus 50 (paragraph 0050 and figure 4)],** a second processor on a second clock connected to the second processor bus as **[a second processor P2 that also has a processor bus 50 (paragraph 0050 and figure 4) the second processor P2 on its own clock domain, P2 clock (paragraphs 0046 and 0056)],** a second direct memory access unit with an external direct memory access channel, and connected to the second processor bus as **[DMA 54, with external interface 55, is connected to the processor bus 50 via interface 57 (paragraph 0052 and figure 4)],** a second programmable unit comprising a second processor interface, the second programmable unit coupled, via the second external direct memory access channel, to the second direct memory access unit, the second programmable unit being programmable by the second processor via the second processor interface as **[access unit 48, connected to DMA 54 via its external**

interface 55 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045) where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)] and a second shareable unit being connectable to the second processor bus as [shareable unit 53 connected to the processor bus 50 (figure 4)], wherein the first programmable unit and the second programmable unit each comprise a processor interface, and a direct access unit core as [the access unit comprises a processor interface, a direct access unit (DAU), and external DMA channel interface (paragraph 0045 and figure 3)] and wherein a first bi-directional communication channel is established between the first shareable unit and the second processor via the first programmable unit, and a second bi-directional communication channel is established between the second shareable unit and the first processor via the second programmable unit as [a communication channel for transferring information can be established between the first shareable unit and the second processor and between the second shareable unit and the first processor (paragraph 0051), access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) and access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4), which can each be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045)].

Koch does not explicitly teach wherein the first programmable unit and the second programmable unit each comprise two external direct memory access channel interfaces, however.

Tang teaches wherein the first programmable unit and the second programmable unit each comprise two external direct memory access channel interfaces as **[a first DMA channel interface for participating in a first DMA transfer, and a second DMA channel interface providing a DMA channel request for a next DMA transfer (column 2, lines 42-55)]**.

Koch and Tang are analogous art, as they are within the same field of endeavor, namely instruction processing, and DMA control.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the dual DMA channel interfaces taught by Tang in each of the programmable units taught by Koch, including using the clock domain of each associated processor for the associated DMA interfaces.

The motivation for doing so, as provided by Tang, would have been **[the second DMA channel interface provides a DMA channel request for a next upcoming DMA transfer, before the current DMA transfer is completed, and initiating set up of the second transfer before the completion of the first, to reduce the latency due to set up time between DMA transfers (column 2, lines 42-55)]**.

As per claim 2, Koch teaches wherein the first and/or second bi-directional channels are half-duplex channels or full-duplex channels as **[the access unit 48**

provides a half-duplex channel to and from the processor bus 40 and the DMA unit 54 (paragraph 0055)].

As per claim 3, Koch teaches wherein both processors are similar from an architectural point of view as **[processors P1 and P2 are similar from an architectural point of view (claim 2)].**

As per claim 4, Koch teaches wherein the processors are implementations of the same type of processor design as **[processors P1 and P2 are implementations of the same type of processor design (claim 3)].**

As per claim 5, Koch teaches wherein the processors are implementations of different types of processor design as **[processors P1 and P2 are implementations of different types of processor design (claim 4)].**

As per claim 6, Koch teaches wherein the shareable unit is a memory, a peripheral, an interface, an input device or an output device as **[examples of shareable units are: volatile memory, non-volatile memory, peripherals, interfaces, input devices, output devices, and so forth (paragraph 0044)].**

As per claim 7, Koch teaches wherein one of the two processors is a CPU, a microprocessor, a DSP, a system controller, a co-processor or an auxiliary processor as

[the processors described can be any of the following: a CPU, a microprocessor, a DSP, a system controller, a co-processor, an auxiliary processor, and so forth (paragraph 0043)].

As per claim 9, Koch teaches wherein the processor interface has a programming link for either connecting to a corresponding processor bus or for connecting to a corresponding processor as **[the access unit has a data link 33 and a control link 34 for connection to the processor bus (paragraph 0045 and figure 3)].**

As per claim 10, Koch teaches wherein the first and second bi-directional communication channels transfer data and/or control information to and from the first and second shareable units via the communication channels as **[each communication channel is employed for transferring data and/or control information to and from the shareable units (claim 11)].**

As per claim 15, Koch teaches an external channel of the first DMA unit to operate on the first processor clock as **[DMA 41, with external interface 42, is connected to processor bus 40 via interface 44 (paragraph 0051 and figure 4) associated with the first processor clock domain, P1 clock (paragraphs 0046 and 0056)];** an external channel of the second DMA unit to operate on the second processor clock as **[DMA 54, with external interface 55, is connected to the processor bus 50**

via interface 57 (paragraph 0052 and figure 4) associated with the second processor clock domain, P2 clock (paragraphs 0046 and 0056)); and a second programmable unit coupled between an external channel of the first DMA unit and an external channel of the second DMA unit as [access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045) where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)], the second programmable unit comprising the second programming interface to the first processor, the second programmable unit also configured to decouple the second processor clock from the first processor clock as [access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045) where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048) and where the access units 48 and 51 decouple the data flow between the clock domain of the first processor and the clock domain of the second processor (paragraph 0056)].

Koch does not explicitly teach wherein each DMA unit comprises two external channel interfaces, however.

Tang teaches wherein each DMA unit comprises two external channel interfaces as **[a first DMA channel interface for participating in a first DMA transfer, and a second DMA channel interface providing a DMA channel request for a next DMA transfer (column 2, lines 42-55)]**.

Koch and Tang are analogous art, as they are within the same field of endeavor, namely instruction processing, and DMA control.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the dual DMA channel interfaces taught by Tang in each of the programmable units taught by Koch, including using the clock domain of each associated processor for the associated DMA interfaces.

The motivation for doing so, as provided by Tang, would have been **[the second DMA channel interface provides a DMA channel request for a next upcoming DMA transfer, before the current DMA transfer is completed, and initiating set up of the second transfer before the completion of the first, to reduce the latency due to set up time between DMA transfers (column 2, lines 42-55)]**.

As per claim 17, Koch teaches an external channel of the first DMA unit to operate on the first processor clock as **[DMA 41, with external interface 42, is connected to processor bus 40 via interface 44 (paragraph 0051 and figure 4) associated with the first processor clock domain, P1 clock (paragraphs 0046 and 0056)]**; an external channel on the second DMA unit to operate on the second processor clock as **[DMA 54, with external interface 55, is connected to the**

processor bus 50 via interface 57 (paragraph 0052 and figure 4) associated with the second processor clock domain, P2 clock (paragraphs 0046 and 0056)); an external channel of the common programmable unit, the external channel to operate on the second processor clock, and the external channel also coupled to the other external channel of the second DMA unit as **[DMA 54, with external interface 55, is connected to the processor bus 50 via interface 57 (paragraph 0052 and figure 4) associated with the second processor clock domain, P2 clock (paragraphs 0046 and 0056)];** an external channel of the common programmable unit, the external channel to operate on the first processor clock, and the external channel also coupled to the second external channel of the first DMA unit as **[DMA 41, with external interface 42, is connected to processor bus 40 via interface 44 (paragraph 0051 and figure 4) associated with the first processor clock domain, P1 clock (paragraphs 0046 and 0056)];** and a second programmable core of the common programmable unit, the second programmable core to operate on the first processor clock as **[the clock signal of the first processor P1 (P1 clock) is fed via a clock line 74 to the DAU core 61 and the processor interface 62 of the access unit 48 (paragraph 0056)],** the second programmable core coupled between the third and fourth external channels of the common programmable unit and the second programmable core comprising the second programming interface to the first processor as **[access unit 48 is connected to processor P1 via processor interface 62 (paragraph 0056) which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)].**

Koch does not explicitly teach wherein each programmable unit and DMA unit comprises two external channel interfaces, however.

Tang teaches wherein each programmable unit and DMA unit comprises two external channel interfaces as **[a first DMA channel interface for participating in a first DMA transfer, and a second DMA channel interface providing a DMA channel request for a next DMA transfer (column 2, lines 42-55)]**.

Koch and Tang are analogous art, as they are within the same field of endeavor, namely instruction processing, and DMA control.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the dual DMA channel interfaces taught by Tang in each of the programmable units taught by Koch, including using the clock domain of each associated processor for the associated DMA interfaces.

The motivation for doing so, as provided by Tang, would have been **[the second DMA channel interface provides a DMA channel request for a next upcoming DMA transfer, before the current DMA transfer is completed, and initiating set up of the second transfer before the completion of the first, to reduce the latency due to set up time between DMA transfers (column 2, lines 42-55)]**.

Response to Arguments

8. Applicant's arguments filed 14 August 2008 have been fully considered but they are not persuasive.

9. Applicant argues that Koch does not teach where the programmable units are programmable by a processor via the processor interface.

However, Koch teaches access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045), where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048), and similarly for access unit 48 and the second processor.

10. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

11. Applicant also argues that Koch does not teach programmable interfaces on cores that have multiple channels to decouple two clock domains.

However, Koch teaches access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045), where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and

0048), and similarly for access unit 48 and the second processor, where the access units 48 and 51 decouple the data flow between the clock domain of the first processor and the clock domain of the second processor (paragraph 0056).

Conclusion

12. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**: claims 8, 11 and 12 have been cancelled, claims 1-7, 9, 10 and 13-22 are rejected.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Nair (US 5890013) - teaches an inter-processor communication system in which each processor has private data and program busses, and these busses are connected to shared memory banks which can be switched between processors.

b. Sunahara (US 5093780) - teaches an inter-processor communication system where each processor writes communication information to a shared memory, and a data link controller transfers data to a memory attached to a second processor automatically.

15. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

16. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 CFR 1.111(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GEORGE D. GIROUX whose telephone number is (571)272-9769. The examiner can normally be reached on Monday through Friday, 9:30am - 6:00pm E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/George D Giroux/
Examiner, Art Unit 2183